Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A device for associating indexes to addresses chosen from among a greater number of values than the number of available indexes, including:

a memory having a plurality of memory locations, each memory location containing ~~indexes~~ at least one index and one respective check ~~words~~ word, the check word of each index being equal to a first set of ~~corresponding to~~ bits having first predetermined positions in the ~~addresses~~ address that is to be associated with ~~the~~ said indexes;

a packing circuit for receiving a current address and for providing a packed address equal to a second set of bits having second predetermined positions in the current address, said first and second predetermined positions being distinct, ~~suppressing in this address bits having said predetermined positions, the~~ said packed address ~~provided by the packing circuit~~ used to select in a read mode a memory location; and

a comparator ~~configured to indicate~~ for comparing the check word of said selected memory location to a third set of bits having said first predetermined positions in the current address, and for indicating that the current address corresponds to the selected memory location when the ~~bits of the~~ check word of the selected location ~~are~~ is equal to the ~~corresponding~~ third set of bits ~~of the current address~~.

2. (Previously Presented) The device of claim 1, wherein the device includes a mask circuit that, according a predetermined mask, annuls bits other than those suppressed by the packing circuit, which also correspond to check word bits.

3. (Original) The device of claim 1, wherein each memory location contains an enable bit indicating whether the location is occupied or not.

4. (Original) The device of claim 1, wherein the addresses are ATM network addresses, and the indexes identify connections of the device to one or several ATM networks.

5. (Previously Presented) The device of claim 4, wherein the addresses provided by the packing circuit have a 16-bit size, the indexes have a 10-bit size, and the check words correspond to the twenty most significant bits of the ATM addresses.

6. (Previously Presented) The device of claim 5, further comprising an input configured to be connected to sixteen ATM networks, the addresses provided to the device having four most significant bits enabling identification of the corresponding ATM networks.

7. (Currently Amended) An address association device, comprising:

a masking circuit configured to receive a plurality of address bits and mask the address bits in accordance with a predetermined mask pattern;

a packing circuit configured to receive address bits from the masking circuit and to reduce the number of address bits to a plurality of index bits and to suppress from the address bits a plurality of check word bits having first predetermined positions in the address bits according to a predetermined packing pattern;

a memory configured to receive the plurality of index bits and the plurality of check word bits and to associate the received index bits and check word bits with ~~the~~ a memory location of a network connection, the memory location containing at least one index and one respective check word, the respective check word of each index being equal to a first set of bits having the first predetermined positions, the packed address equal to a second set of bits having second predetermined positions in the address bits, the first and second predetermined positions being distinct; and

a comparator coupled to the memory and configured to receive the plurality of address bits and to compare the check word of the selected memory location to a third set of bits having the first predetermined positions, and to indicate when selected bits from the plurality of

address bits correspond to the plurality of check word bits associated with the memory location addressed in the plurality of address bits.

8. (Original) The device of claim 7 wherein the masking circuit is configured by the predetermined mask pattern to mask bits not suppressed by the packing circuit when the number of bits used to address a network connection in memory is fewer than the number of bits remaining after the plurality of address bits are reduced by the packing circuit.

9. (Original) The device of claim 7 wherein each network connection in memory includes an enable bit that is configured to signal when the network connection in memory is an active connection to the network.

10. (Previously Presented) The device of claim 9, further comprising a logic circuit coupled to the enable bit and to the comparator and configured to indicate when a selected location addressed by the plurality of address bits is an active location.

11. (Previously Presented) The circuit of claim 7, further comprising a register configured to store a base address corresponding to a beginning address in memory and, further comprising an adder for adding the base address to the address bits received from the packing circuit.

12. (Currently Amended) A method for associating ~~addresses~~ an address to a memory location ~~locations~~, comprising:

receiving a plurality of address bits and masking the address bits in accordance with a predetermined mask pattern;

packing the masked plurality of address bits to reduce the number of address bits to a plurality of packed address bits according to a predetermined packing pattern and suppressing check word bits from the masked address bits, the check word bits having first predetermined positions in the plurality of address bits, the memory location containing at least

one index and one respective check word, the respective check word of each index being equal to a first set of bits having the first predetermined positions, the packed address equal to a second set of bits having second predetermined positions in the address bits, the first and second predetermined positions being distinct;

associating the packed bits with a memory location corresponding to a network connection; and

comparing the check word of the selected memory location to a third set of bits having the first predetermined positions, ~~selected bits from the plurality of address bits for a selected memory location with selected bits associated with a memory location addressed in the plurality of address bits~~ and indicating when there is a match.

13. (Original) The method of claim 12 wherein masking comprises configuring the predetermined masking pattern to mask bits not suppressed by packing when the number of bits used to address a selected memory location is fewer than the bits remaining after packing.

14. (Original) The method of claim 12, further comprising ANDing an enable bit with the results of the comparing to determine if a selected memory location is an active connection.

15. (Previously Presented) The method of claim 12 wherein packing comprises storing a base address corresponding to a beginning address in memory and the method further comprises adding the base address to the packed address bits reduced during packing.

16. (Canceled)

17. (Previously Presented) The method of claim 14, further comprising disabling an enable bit corresponding to a memory location selected by the plurality of address bits when the memory location is occupied.

18. (Original) The method of claim 17 wherein masking comprises configuring the predetermined mask pattern to mask bits not suppressed by packing when the number of bits used to address a selected memory location is fewer than the bits remaining after packing, and further comprising configuring the predetermined mask pattern to mask bits to prevent accessing selected memory locations that have been previously addressed.

19. (Previously Presented) A device for associating indexes to addresses chosen from among a greater number of values than the number of available indexes, including:

a memory containing indexes and respective check words corresponding to predetermined bits of the addresses associated with the indexes;

a packing circuit receiving a current address and suppressing bits in the current address in accordance with a pattern such that the suppressed bits correspond to bits of the check words and the bits not suppressed from a packed address, the packed address used to select in a read mode a memory location, the packed address provided by the packing circuit having a 16-bit size, the indexes having a 10-bit size, and the check words correspond to the twenty most significant bits of the ATM addresses; and

a comparator configured to indicate that the current address corresponds to the selected memory location when the bits of the check word of the selected location are equal to the corresponding bits of the current address.

20. (Previously Presented) A device for associating indexes to addresses chosen from among a greater number of values than the number of available indexes, including:

a memory containing indexes and respective check words corresponding to predetermined bits of the addresses associated with the indexes;

a packing circuit receiving a current address and suppressing bits in the current address in accordance with a pattern such that the suppressed bits correspond to bits of the check words and the bits not suppressed from a packed address, the packed address used to select in a read mode a memory location, the packed address provided by the packing circuit having a 16-bit size, the indexes having a 10-bit size, and the check words correspond to the twenty most significant bits of the ATM addresses;

a comparator configured to indicate that the current address corresponds to the selected memory location when the bits of the check word of the selected location are equal to the corresponding bits of the current address; and

an input configured to be connected to sixteen ATM networks, the addresses provided to the device having four most significant bits enabling identification of the corresponding ATM networks.

21. (Previously Presented) An address association device, comprising:

a masking circuit configured to receive a plurality of address bits and mask the address bits in accordance with a predetermined mask pattern;

a packing circuit configured to receive address bits from the masking circuit and to reduce the number of address bits to a plurality of index bits and to suppress a plurality of check word bits from the address according to a predetermined packing pattern;

a memory configured to receive the plurality of index bits and the plurality of check word bits and to associate the received index bits and check word bits with the memory location of a network connection; and

a comparator coupled to the memory and configured to receive the plurality of address bits and to indicate when selected bits from the plurality of address bits correspond to the plurality of check word bits associated with the memory location addressed in the plurality of address bits;

wherein the masking circuit is configured by the predetermined mask pattern to mask bits not suppressed by the packing circuit when the number of bits used to address a

network connection in memory is fewer than the number of bits remaining after the plurality of address bits are reduced by the packing circuit.

22. (Previously Presented) A method for associating addresses to memory locations, comprising:

receiving a plurality of address bits and masking the address bits in accordance with a predetermined mask pattern;

packing the masked plurality of address bits to reduce the number of address bits to a plurality of packed address bits according to a predetermined packing pattern and suppressing check word bits from the masked address bits;

associating the packed bits with a memory location corresponding to a network connection; and

comparing selected bits from the plurality of address bits for a selected memory location with selected bits associated with a memory location addressed in the plurality of address bits and indicating when there is a match; wherein masking comprises configuring the predetermined masking pattern to mask bits not suppressed by packing when the number of bits used to address a selected memory location is fewer than the bits remaining after packing.